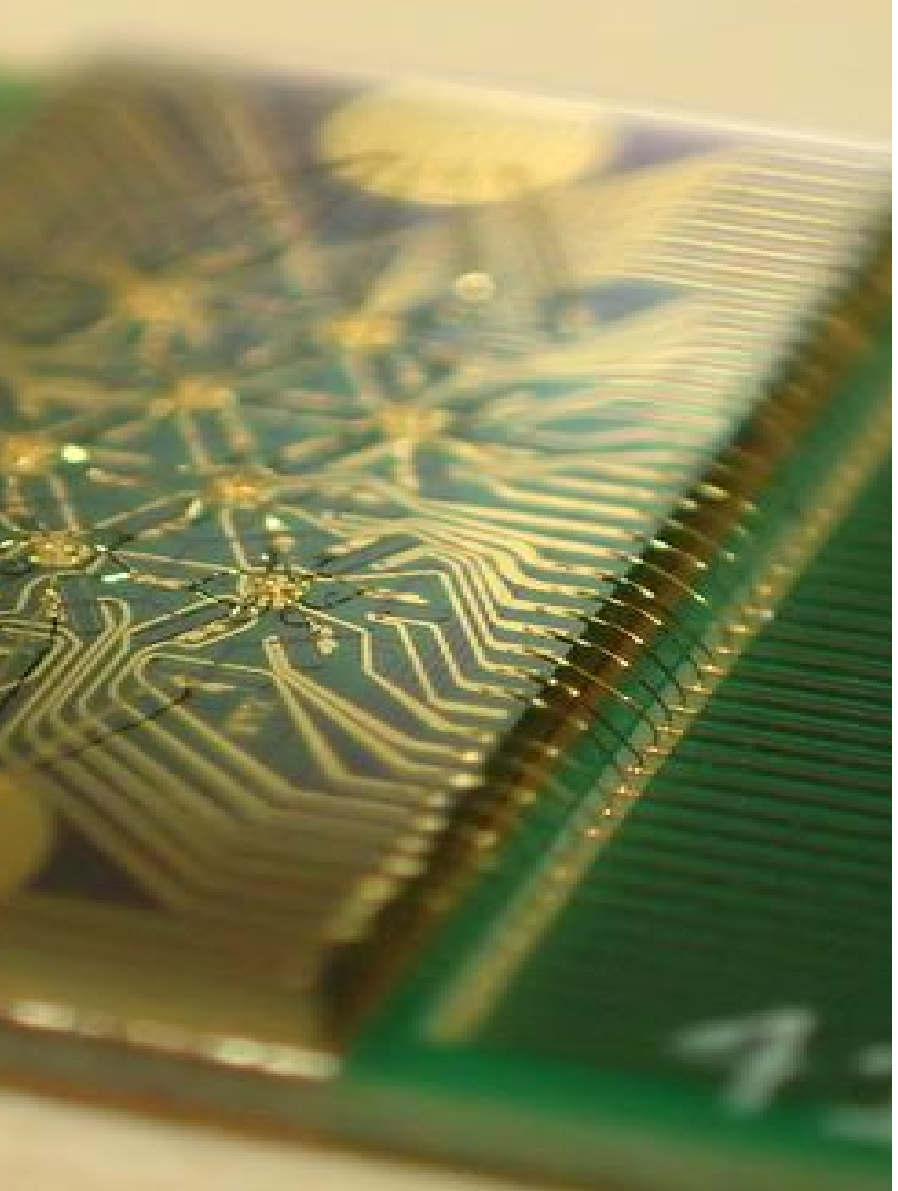


30/09/19

Iñigo Artundo

PIC industry overview

Design and test trends

PHOTONIC INTEGRATION CONFERENCE

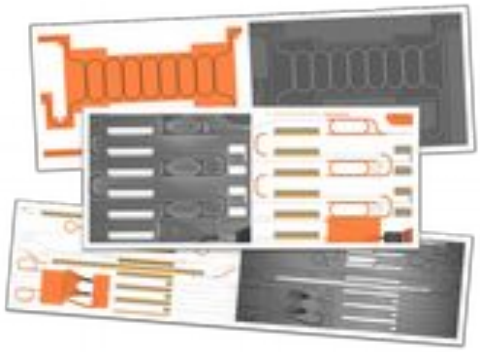
VLC PHOTONICS

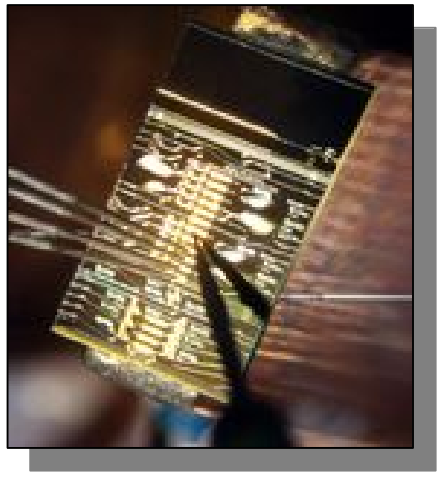
Who we are

- 14-people team of extensive technical and business experience.
- Located in Valencia, Spain.
- Company founded in 2011.
- 14+ years in the field of integrated photonics.

Our business

Provide engineering services for the development of

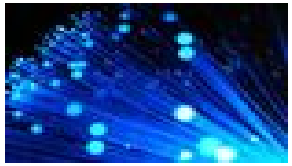




Photonic Integrated Circuits

Fabless design and test house

Where are PICs now?



Communications

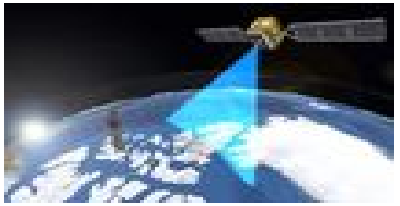
- Optical Datacom
- Telecom access (xPON)
- Microwave/RF/THz Photonics, 5G
- Long-haul & transport networks

Sensing

- Fiber sensor interrogators
- Gyroscopes
- Spectroscopy
- Interferometry

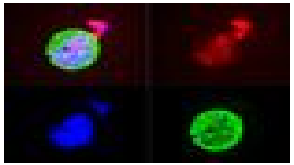
Signal Processing

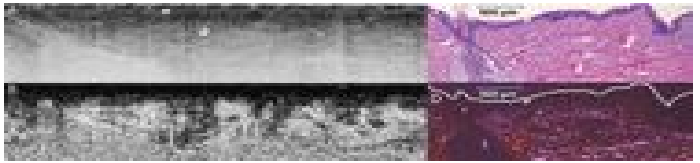
- Artificial Intelligence
- Beamforming/steering/LIDAR
- Astrophotonics
- Quantum Optics



BioPhotonics

- Medical Instrumentation
- Photonic Lab-on-a-Chip
- Analytics and Diagnostics
- Optical Biosensors

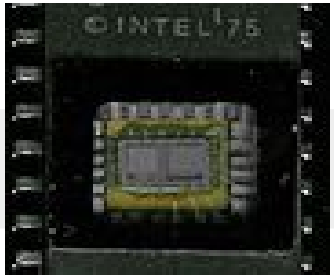




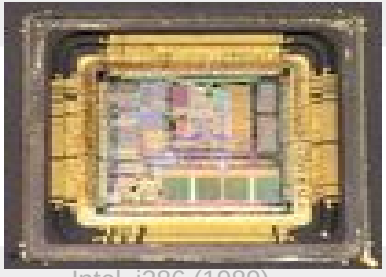
Where is photonic integration now?

'10 '00 '90 '80 '70 '60

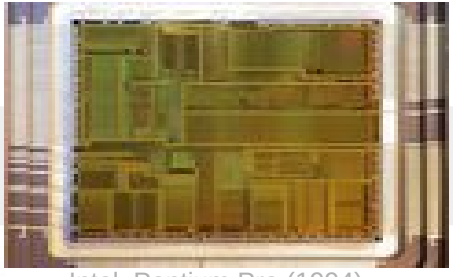
Jack Kilby, Texas Instruments (1958)



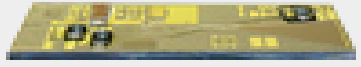
Intel. B2708-1 (1975)



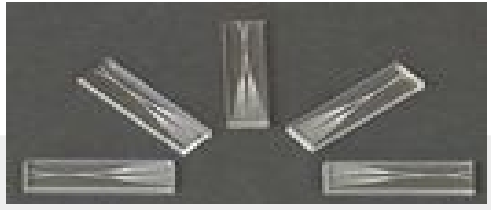
Intel. i386 (1989)



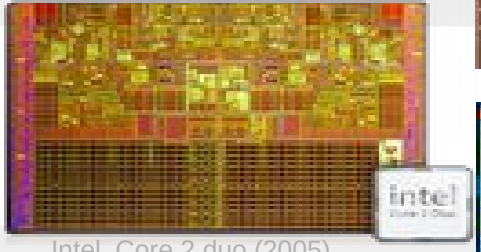
Intel. Pentium Pro (1994)



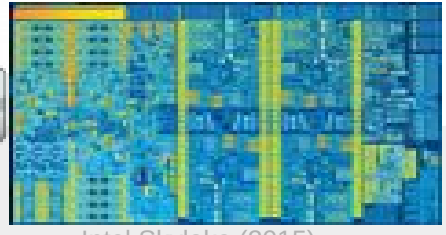
Coherent PIC



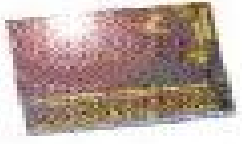
PLC splitters and AWGs



Intel. Core 2 duo (2005)



Intel Skylake (2015)



Infinera 100G PIC (2005)

<2k blocks

IBM 100G SiPhot PIC (2015)

Where is photonic integration now?

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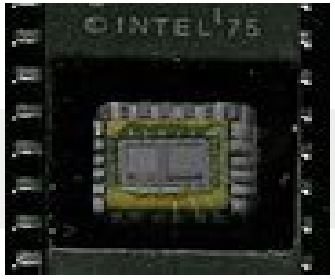

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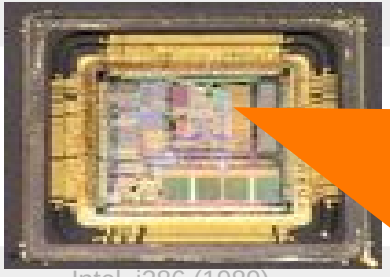

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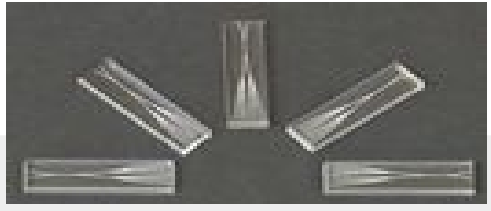
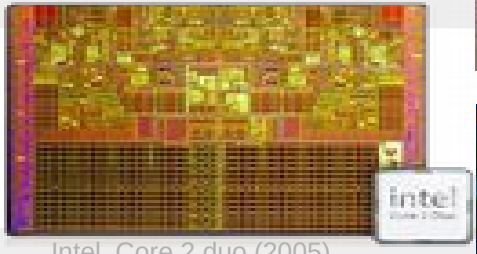


PLC splitters and AWGs



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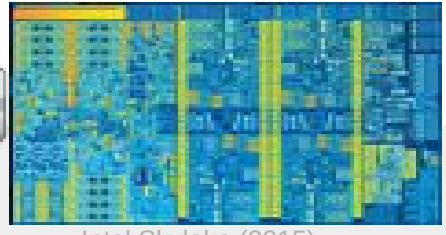


Intel Skylake (2015)

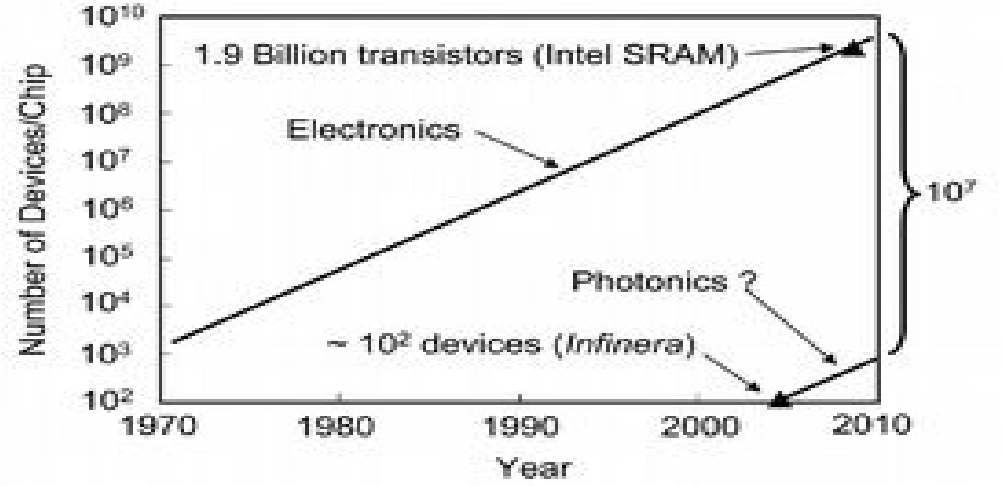
+30 years behind!

Infinera 100G

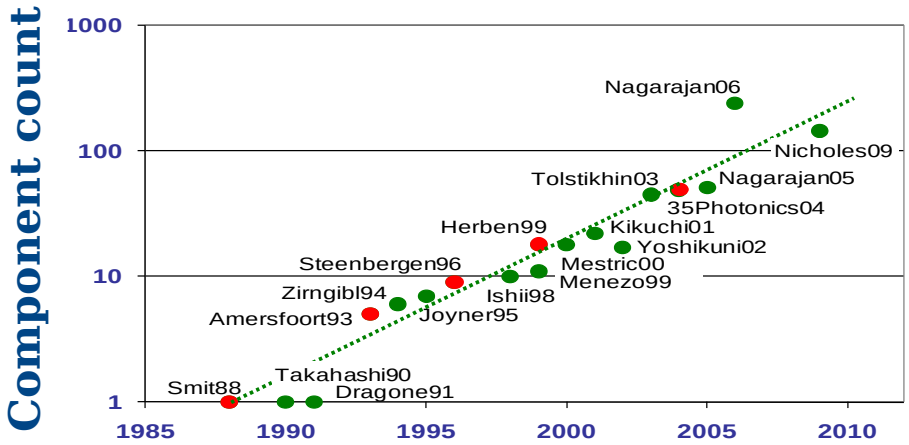
<2k blocks

IBM 100G SiPhot PIC (2015)

Manufacturing scalability



I.P. Kaminow, "Optical Integrated Circuits: A Personal Perspective," J. Lightwave Technol. Vol. 26, no. 9 pp. 994-1004 (2008)



Courtesy of Prof. M.K. Smit, TU/e, The Netherlands

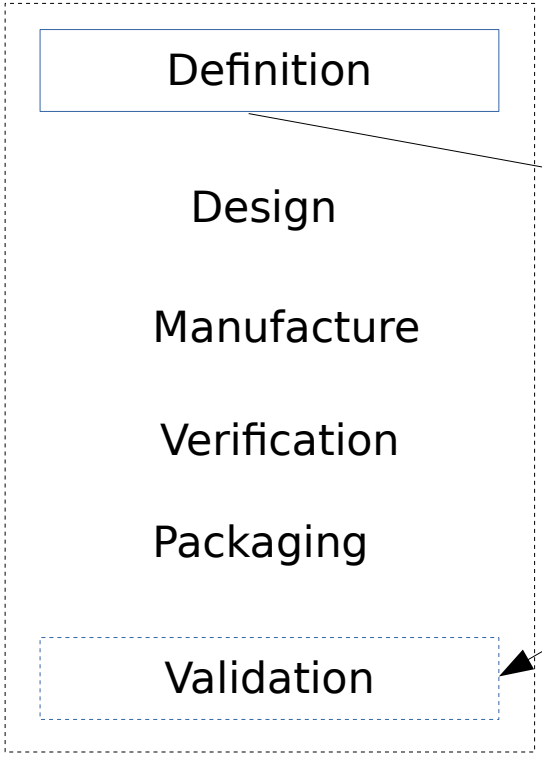
Ultimately, manufacturing scalability is worse than in digital electronics, due to:

1) Several material platforms (Si, InP, PLC, $LiNbO_3$, SiN, etc.)
2) More building block diversity per circuit, and lower circuit complexity
3) Feature size limitation by wavelength

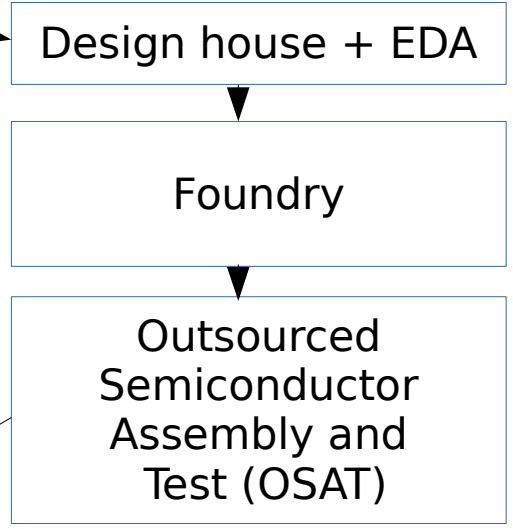
Scaling up affordably

Vertical model

Horizontal model



Fabless model



Working with a design house

COST

- **Engineers contracted only during design phase (10-20% project time).**
  - Not permanently on your payroll.
- **Access to (several) commercial software tools.**
  - Avoid costly software licenses.

TIME TO MARKET

- **Access to design manuals, PDKs, foundry contacts.**
  - Minimize NDA, DKLA, interfacing issues.
- **Experienced designers from day 1.**
  - Spare costly and lengthy training periods.

SUCCESS

- **Wide experience from many projects, tools and material platforms.**
  - Speed up while minimizing risks.
- **Test capabilities and network of foundry and packaging partners.**
  - Simplify supply chain evaluation and interfacing.

Design link to manufacturing

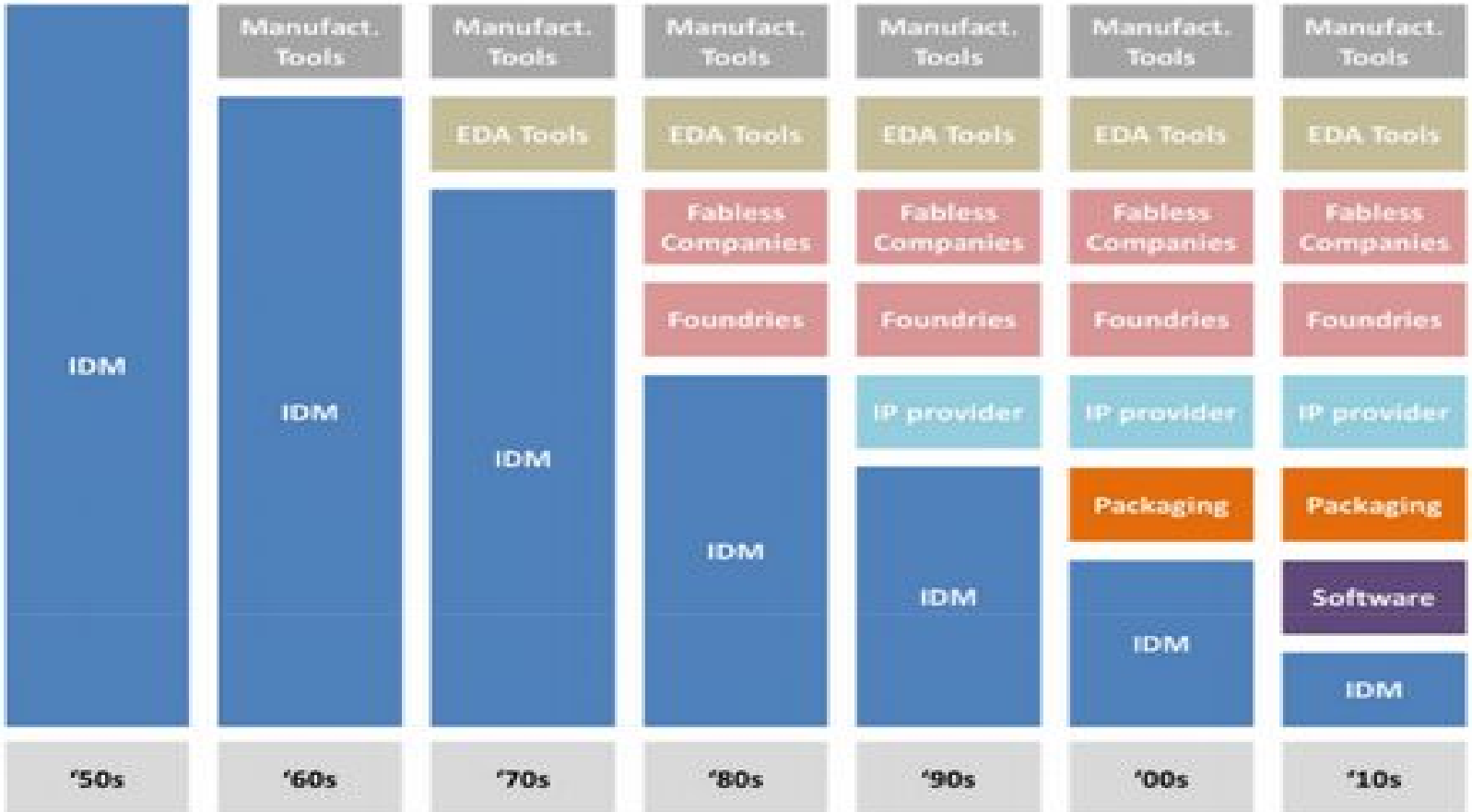
Designs need to target a specific material platform and foundry process.

Selection depends on technical and business criteria.

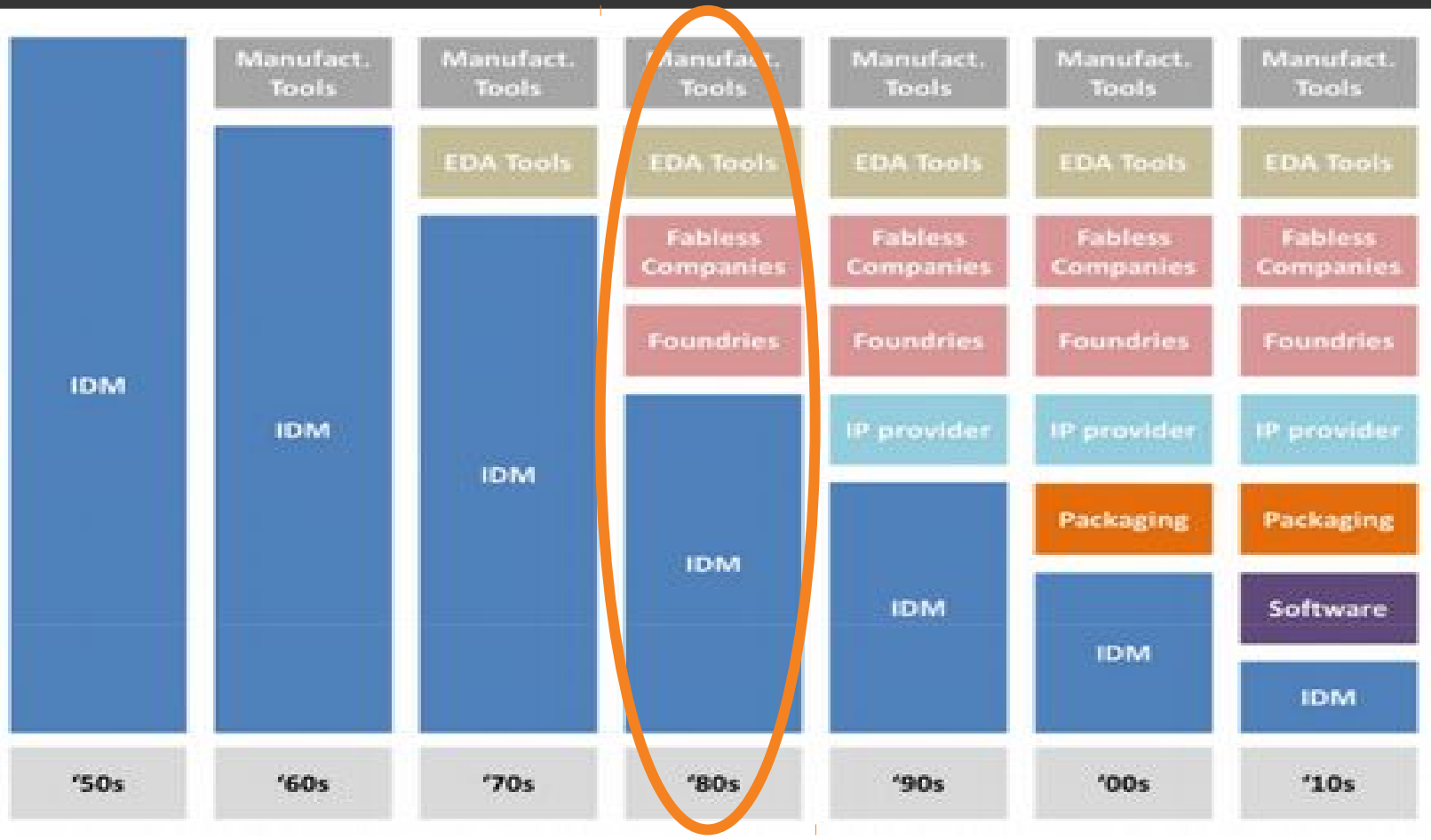
This is a critical choice as portability is challenging.

Photonic foundry landscape is growing and changing quickly.

Semiconductor ecosystem

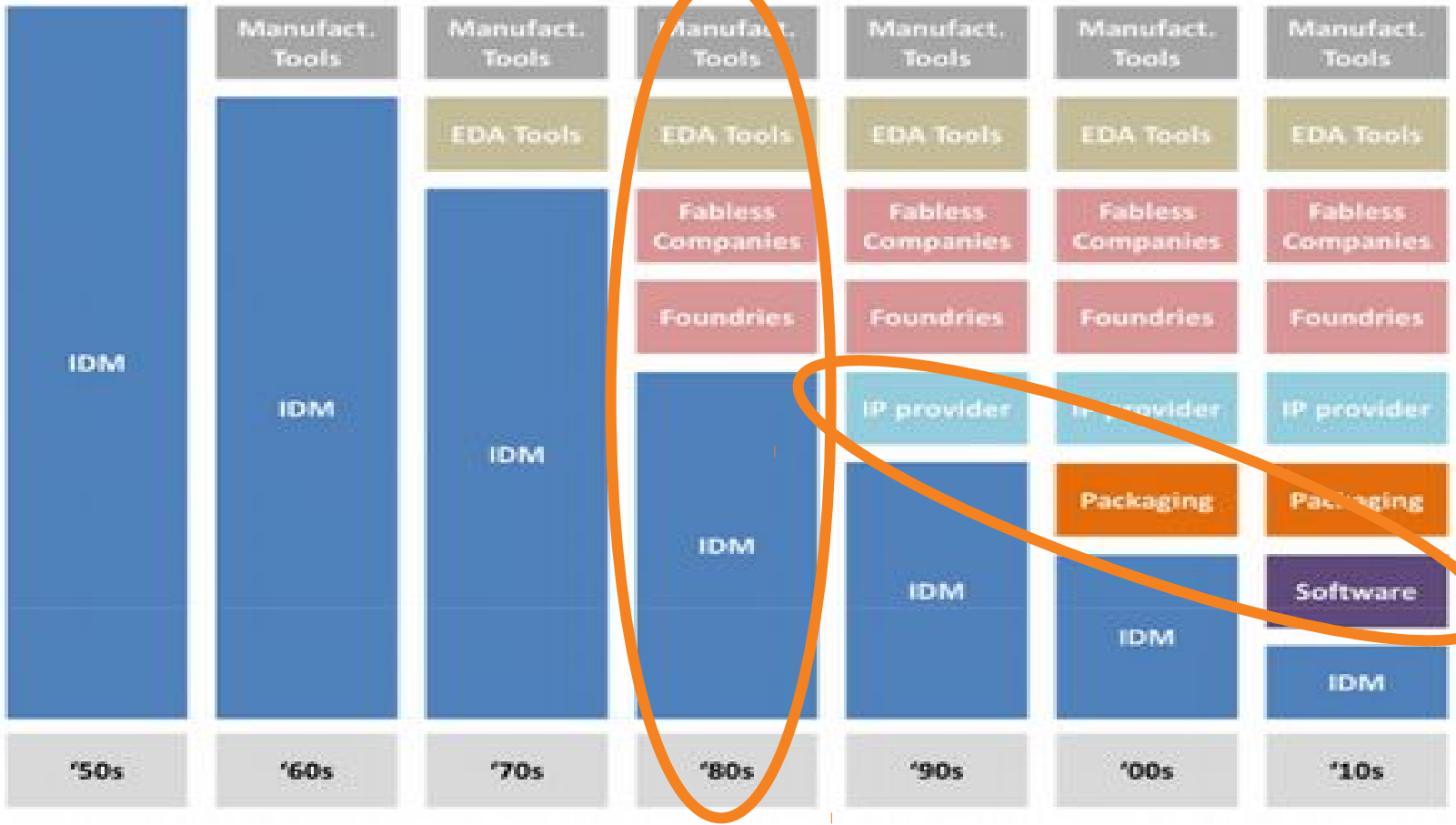


Semiconductor ecosystem



30 years behind!

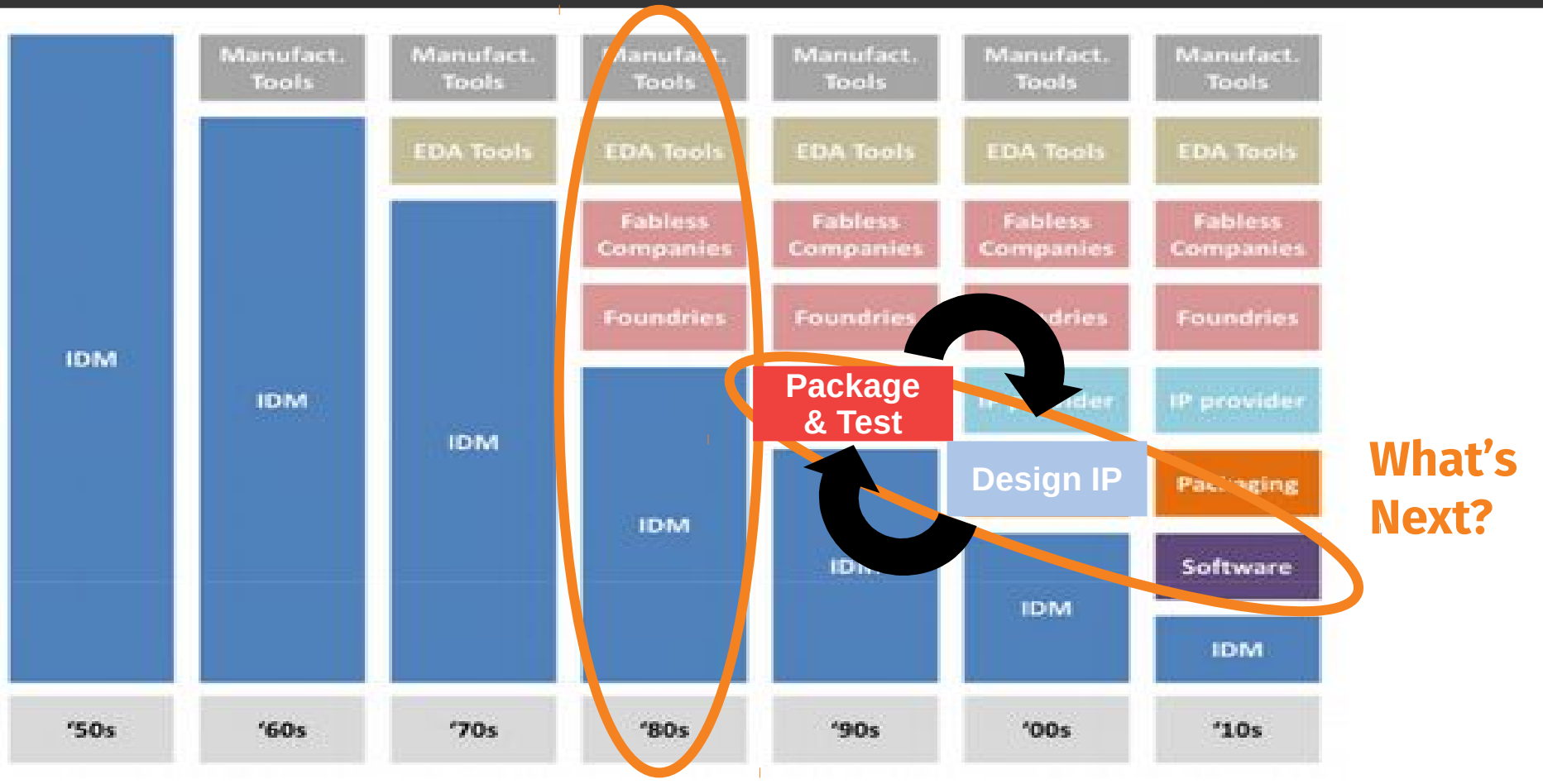
Semiconductor horizontal supply



What's Next?

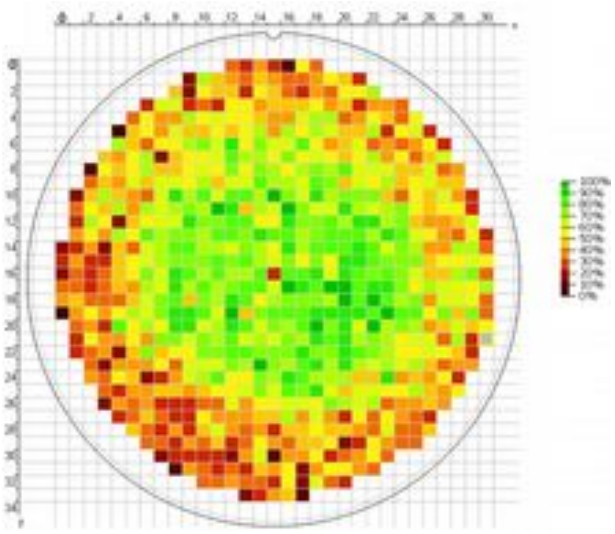
30 years behind!

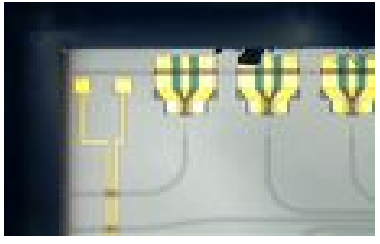
Semiconductor horizontal supply

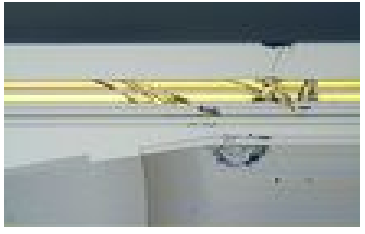


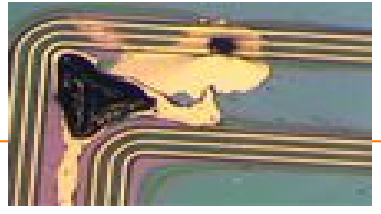
30 years behind!

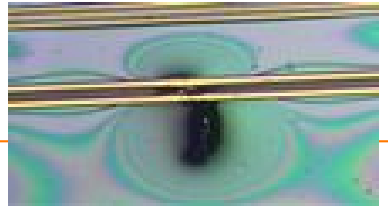
Need for test: design validation

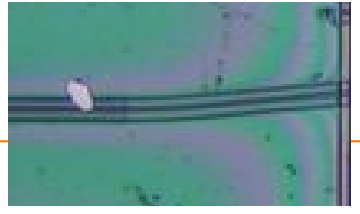












Foundry metrology

- Wafer & epitaxy issues
- Litho, etch & deposit tolerance
- Visual inspection
- Electrical screening
- PCM and PDK performance
- Overall yield

Customer / Test house

- PIC/wafer level characterization
  - Fab process verification
  - Building block validation
  - Circuit validation
- Root cause analysis
- Feedback for design models

Scaling up testing

PROOF OF CONCEPT (1-100 dies)

- MPW runs, manual bare die testing

PROTOTYPING (100 - 1000+ dies, 1-25 wafers)

- Dedicated runs, semi-automated testing

PILOT (25+ wafers) and VOLUME PRODUCTION

- Automated wafer level testing

REQUIREMENTS:

- Facilities (clean room, redundant test stations)
- Equipment (semi/automated alignment stages)
- Instrumentation (OSA/BOSA, OVNA, PARBERT, V-I sources, OTDR...)
- Personnel (highly educated and training)

COST
TIME TO MARKET
RISK

What is Design IP?

- A reusable functional design with a defined interface and behavior that has been verified by its vendor and can be integrated into a larger design.
- This proprietary know-how may be backed by patents, semiconductor topographies, trademarks, copyright and trade-secrets.

An IP block may include:

- Design source code
- GDSII layout (DRC clean)
- Design models and simulations
- Characterization measurement info
- Associated models

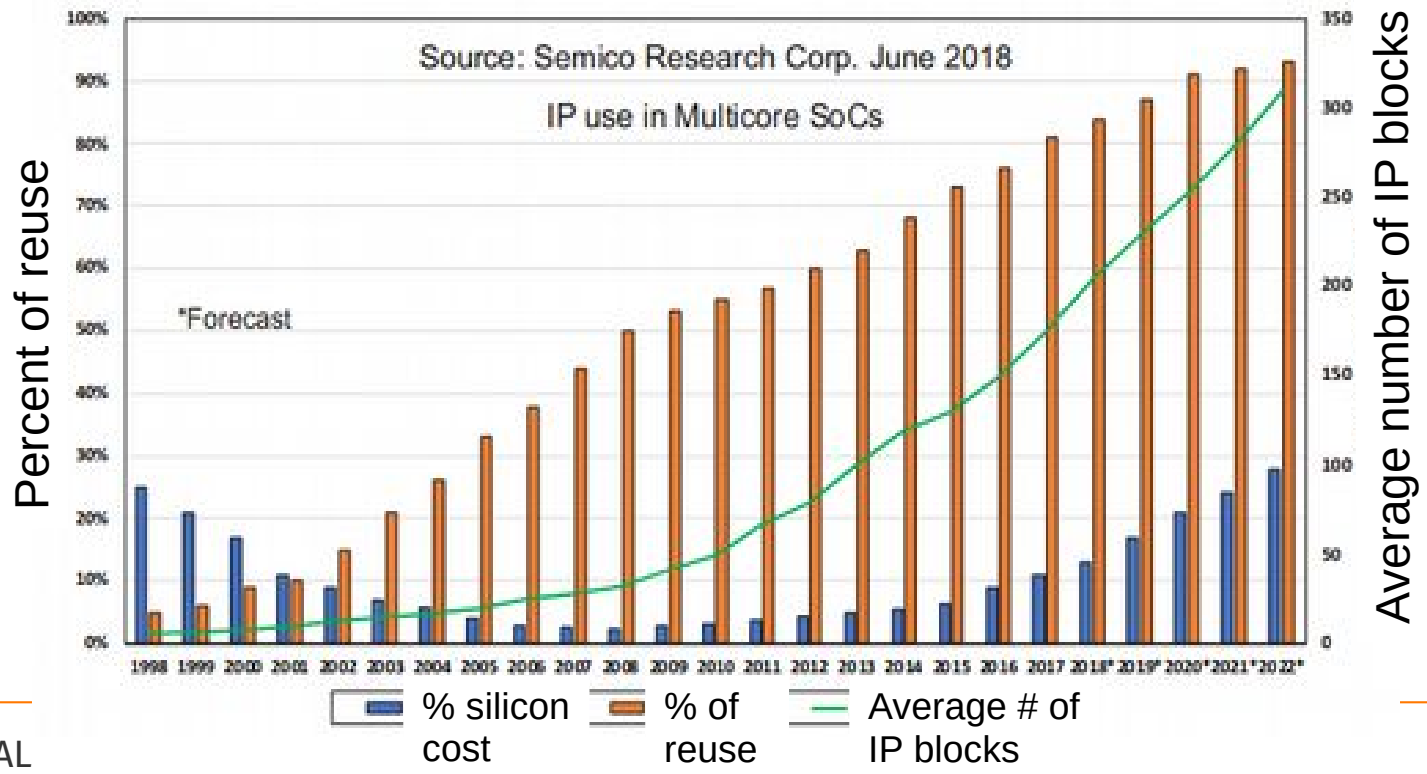
- Target foundry(ies) and processes
- Guarantees
- Export controls
- Versions and releases
- Maintenance and support
- Licensing terms and conditions

Added value of design IP

- **Time to market:** accelerate product development by design reuse and shorten the time to market, launching rapidly.
- **Availability of skilled designers:** it alleviates the need for sophisticated skills, experienced developers and expert knowledge in the target application domains.
- **Development cost:** IP vendors can usually amortize their development risk costs over many customers.
- **Technical risks:** Avoid testing and verification of first time designs, as commercial design IP is usually validated for certain manufacturing processes.
- **Product lifecycle management:** Design support and optimization for users along the whole product lifecycle.
- **Boost performace:** easily increase circuit complexity.
- **Target new applications:** Easy to diversify product portfolios by using new IP.
- **Legal risks:** Internally developed IP may have legal issues, as it may (inadvertently) infringe existing intellectual property rights. Commercial IP is better checked.

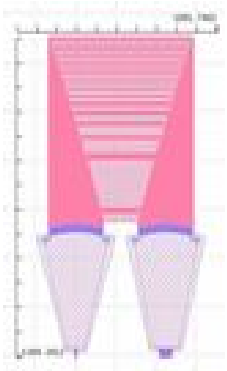
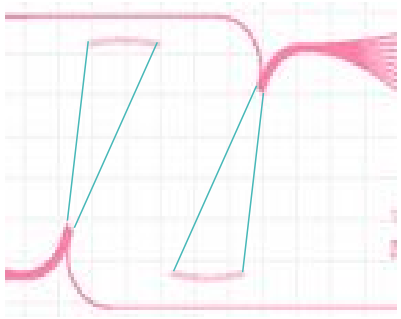
Design IP usage and cost

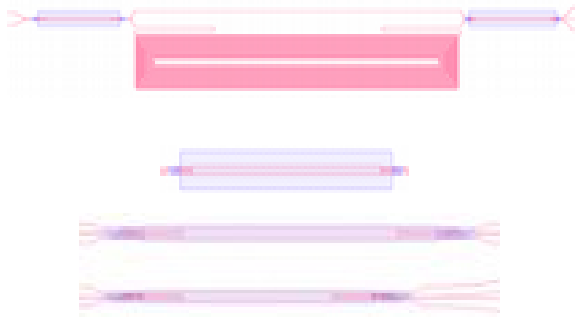
- In ICs there are hundreds of IP blocks being used nowadays in each design.
- IP cost was high when there were few (expensive) blocks and not reused.
- IP cost decreased quickly as reuse increased.
- Total costs increased again, due to the high licensed number of (cheaper) blocks.



VLC Photonics design IP

- Libraries for +10 foundries (SOI, SiN, InP, PLC).
- More than 140 custom building blocks: MMIs, MZIs, AWGs, grating couplers, spirals, crossings, ring resonators, DBRs, directional couplers, Y junctions, inverted tapers, star couplers, waveguide transitions, SOAs, DFB lasers, SG-DBRs, SSCs, switches, modulators, photodetectors, etc.
- Robust design methodology and quality processes.



Design and test challenges

- Poor PDKs (compact models, validated cells/pcells, fab tolerances).
- Mixed Photonic-Electronic co-design.
- Design-for-test, Design-for-packaging.
- Poor circuit verification tools: DRC, LVS.
- Carrier and Package co-design: mechanical/optical/RF/thermal/multi-physics.
- Lack of validation standards for complex PICs.

For all your PIC needs

VLC PHOTONICS

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