Chip- and system-level opto-electronic integration trends

Bert Jan Offrein

Photonics Integration Conference, September 27, 2016
Interconnect trends in DC architectures

- Bandwidth scaling
- Bridge longer distances
- Increase bandwidth density
- Improve power efficiency
- Increase switch port count

- Improve system flexibility

- While massively reducing cost
How can optics help?

- Bandwidth scaling
- Bridge longer distances
- Increase bandwidth density
- Improve power efficiency
- Increase switch port count
- Improve system flexibility
- While massively reducing cost

- Reduce the electrical signal path length
- High density optics
- Scale bandwidth per fiber
- Single mode technology
- Standardized interfaces
- Integration
- Reduce assembly overhead
- Standardization
Outline

- Photonics integration roadmap
- The need for integration at component and system level
- CMOS Silicon photonics
- Scalable silicon photonics packaging
- Summary
High-Level Server System Architecture

Where’s the potential to use optics for adding value and performance?
High-Level Server System Architecture

Server node
- CPU
- PCI extension (Accelerator)
- DRAM & NVM
- Bridge
- NIC
- BMC

Storage node
- Storage controller
- Storage

Backup node
- Management
- (Tape) library controller

Intra DC Network
- Mostly small distances

Inter DC Network
- Mostly small BW

Internet
- Mostly small distances

Mostly small distances

Courtesy Dr. Martin Schmatz

© 2016 IBM Corporation
High-Level Server System Architecture

Accelerators: PCIe, SMP-bus or network attach.

Highest growth potential

Optics to dominate Standards

Courtesy Dr. Martin Schmatz
Photonics integration roadmap (1 of 2)

2008
- Electrical system, optical fibers at card edge only
- IBM Roadrunner

2011
- Optical fibers across the boards
- IBM Power 775

IBM Research - Zurich
Why integration? Looking back, electronics

Today’s state of computing is based on:
- Integration and scaling of the logic functions (CMOS electronics)
- Integration and scaling of the interconnects (PCB technology & assembly)

For optical interconnects, this resembles:
- Electro-optical integration and scaling of transceiver technology
- Integration of optical connectivity and signal distribution

Whirlwind, MIT, 1952

EAI 580 patch panel, Electronic Associates, 1968

Pictures taken at:

Computer History Museum
Photonics technologies for system-level integration

1. **Chip-level: CMOS silicon photonics**

- Si photonics provides all required building blocks (except lasers) on chip-level:
  - Modulators
  - Drivers
  - Detectors
  - Amplifiers
  - WDM filters

  + CMOS electronics

2. **System-level: Optical Printed circuit board technology**

- Provide electrical and optical signal routing capability
- Enable a simultaneous interfacing of electrical and optical connections
- One step mating of numerous optical interfaces
- Avoid fiber cable handling at board or carrier level
Chip-level integration

Opto-electronic chip

Flexible optical waveguides or fibers

Optical waveguides on carrier
CMOS Silicon photonics

Provides the integration of optical and electrical functions

⇒ **Silicon photonics**
- Modulators
- Drivers
- Detectors
- Amplifiers
- WDM filters
- Dense integration
- + CMOS electronics

**CMOS chip cross-section**  **WDM filter**  **Modulator**  **Detector**
4 $\lambda \times 25$ Gb/s optical transceiver demonstration

Demonstration of a flip chip mounted 100G transceiver with four wavelength multiplexing at 25 G each.

Bert Jan Offrein
Integrating the light source

Silicon photonics: Versatile and cost-efficient

- Si: Indirect bandgap → Additional material for laser sources required.
- Today: External laser source → must be coupled.

CMOS embedded III-V–on–silicon platform

Requirements:

- Thin III-V layer (< 500 nm).
- High modal overlap with active material (low-power consumption, high-speed modulation).

Yet, III-V–on–silicon devices cannot be fully integrated (device thickness ~ 3…4 µm).

Hybrid

State-of-the-art

Semi-Hybrid
demonstrated

Monolithic

Our research focus
CMOS embedded III-V–on–silicon platform

- Monolithically integrated functionalities
  - Directly modulated lasers
  - Tunable lasers
  - Laser arrays
  - Wavelength/power stabilization
  - ...

- Cost advantages
  - Lasers at the cost of silicon
  - Reduced packaging overhead

CMOS embedded III-V cross section

III-V on silicon chip
H2020 EU project DIMENSION
System-level integration

Flexible optical waveguides

Opto-electronic chip or fibers

Optical waveguides on carrier
From Si photonics transceivers to chip-level assembly

Treat Si photonics chip as a Si ASIC → Need optical interface at carrier-level

- Less components and assembly steps
- Improved electrical signal path, reduce number of interfaces and signal distance
- High density, scalable optical IO
- Minimum overhead, lowest cost

Similar technology applicable for Si photonics subassemblies for transceivers
Adiabatic optical coupling using polymer waveguides

- Contact between the silicon waveguide taper and the polymer waveguide (PWG), achieved by flip-chip bonding, enables adiabatic optical coupling.

Schematic view of assembled Si photonics chip by flip-chip bonding.
Optical printed circuit board technology

**Waveguide processing:**
- Use of liquid, UV-sensitive, low-loss polymers with high environmental stability
- Large-panel processing with short processing time
- PCB-fabrication compatibility

**Polymer deposition**
- ① Polymer bead
- ② Speed \( v = \text{const.} \)
- ③ Polymer layer

**Waveguide patterning**
- Highly-collimated Hg(Xe) lamp with 20 x 20 cm exposure field
- Sequential UV laser writing into polymer

Bert Jan Offrein
Single-mode polymer waveguide technology

SM polymer waveguides on **chips** (e.g. Si photonics chips)

SM polymer waveguides on **panel-size flexible** substrates

SM polymer waveguides on **wafer-size flexible** substrates

---


Bert Jan Offrein
Optical characterization scheme

- Light coupled to PWGs by SM optical fiber
- Optical loss per coupler
- Variation of total taper length and wavelength sweep

Microscope picture through the glass substrate
Adiabatic couplers PWG direct processing

- New design and processing
  - Larger silicon waveguide bending radius
  - Higher resolution e-beam writing

- For a taper length >1.6 mm:
  - Coupling loss TE<1 dB & TM < 0.5 dB @ 1310 nm
Operation across the O and the C band

- The adiabatic couplers operate across the O and C band
  - The TM mode is leaking to the silicon substrate in the C band
Waveguide to fiber connection through a Si V-groove array

- Different assemblies were realized with Si-adapter glued to transparent substrates
- Coupling loss to fibers below 0.5 dB demonstrated
Photonics integration roadmap (2 of 2)

**TODAY:** Current research focus: E-O integration on carrier level

**Vision:** E-O integration on chip level

- Opto-electronic chip
- Flexible optical waveguides or fibers
- Optical waveguides on carrier
- Optical transceiver integrated with the processor
- Optical waveguides in/on boards

- Processor
- Fibers
Acknowledgements

• Collaborators in IBM
  – And many others

• Dow Corning

• European Union co-funded projects

Dow Corning

DIMENSION

RAPIDO

CarriCool

ADDAPT
Summary

• Chip level integration of silicon photonics onto the processor package
  – Offers a path to high bandwidth and low cost optical IO
  – A supply chain ecosystem has to be established

• CMOS Silicon photonics and integration path for III-V materials

• Multimode and single mode polymer waveguide technology demonstrated
  – Based on silicone materials from Dow Corning

• Adiabatic optical coupling enables efficient, broadband and polarization independent chip to polymer waveguide interfacing
  – Compatible with existing electrical assembly processing steps

• Polymer waveguide to fiber interface based on a Si V-groove adapter

Path towards high level of electro-optical integration & scalability
Thank you for your attention

- Bert Jan Offrein
- ofb@zurich.ibm.com